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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Lukas P.P.P. van Ginneken		
Title:	Timing Closure Methodology		
Application No.:	10/828,547	Filing Date:	April 19, 2004
Examiner:	Unassigned	Group Art Unit:	2825
Docket No.:	MDAI.001US3	Conf. No.:	3884

Certificate of Mailing Under 37 CFR 1.8

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Mary E. Buggie

Mary E. Buggie

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

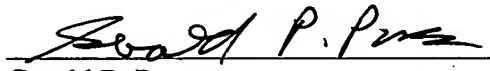
Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicants call the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 are enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664. This form is being submitted in duplicate.

Respectfully submitted,



October 6, 2005

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U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	MDAI.001US3	10/828,547
	Applicant	**Conf. No.**
(Use several sheets if necessary)	Lukas P.P.P. van Ginneken	3884
(Form PTO-1449)	**Filing Date**	**Art Group**
	April 19, 2004	2825

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	1	Berkelaar et al., "Gate Sizing in MOS Digital Circuits With Linear Programming", The European Design Automation Conference, March 12-15, 1990, pp. 217-221.
	2	Chuang et al., "Delay and Area Optimization for Discrete Gate Sizes Under Double-Sided Timing Constraints", Proc. IEEE 1993 Custom Integrated Circuits Conf., pp. 1-4.
	3	Chuang et al., "Timing and Area Optimization for Standard-Cell VLSI Circuit Design", IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 3, March 1995, pp. 308-320.
	4	Marek-Sadowska et al., "Timing Driven Placement", IEEE, 1989, pp. 94-97.
	5	Conn et al., "Optimization of Custom MOS Circuits by Transistor Sizing", Proceedings of the 1996 IEEE/ACM International Conference on Computer-Aided Design, November 10-14, 1996, pp. 174-180.
	6	Youssef et al., "Bounds on Net Delays for VLSI Circuits", IEEE Transaction on Circuits and Systsms-II: Analog and Digital Signal Processing, Vol. 39, No. 11, November 1992, pp. 815- 824.
	7	Avant!, "Solar™ A Physical Optimization Tool for Deep Submicron IC Layout", 1996, 4 pages.
	8	Coudert, Olivier, "Gate Sizing: A General Purpose Optimization Approach", IEEE, 1996, 5 pages.
	9	Jackson, et al., "Performance-Driven Placement of Cell Based IC's", 26th ACM/IEEE Design Automation Conference, Paper 24.2, 1989, pp. 370-375.
	10	Kim, et al., "Concurrent Transistor Sizing and Buffer Insertion by Considering Cost-Delay Tradeoffs", ISPD, ACM, 1997, pp. 130-135.
	11	Lillis, et al., "Optimal Wire Sizing and Buffer Insertion for Low Power and a Generalized Delay Model", IEEE Journal of Solid-State Circuits, Vol. 31, No. 3, March 1996, pp. 437-447.
	12	Lin et al., "Logic Synthesis for Engineering Change", 32nd ACM/IEEE Design Automation Conference, 1995, 6 pages.
	13	Luk, Wing K., "A Fast Physical Constraint Generator for Timing Driven Layout", 28th ACM/IEEE Design Automation Conference, Paper 37.3, 1991, pp. 626-631.
	14	Chan, Pak K., "Algorithms for Library-Specific Sizing of Combinational Logic", 27th ACM/IEEE Design Automation Conference, Paper 21.4, 1990, pp. 353-356.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.